

MC13192/13193 Errata

2.4 GHz Low Power Transceiver for 802.15.4

1 Introduction

This errata pertains to MC13192/13193 V2.3 engineering samples and target IC Data Sheet, MC13192/13193, and Reference Manual, MC13192RM. This document is included in shipments for which this errata applies. These errata pertain to devices which have been shipped with date code marking 4442 or later.

2 Version 2.3 Errata

Table 1. Version 2.3 Errata Details

No	Errata	Work Around
1	If a new interrupt event occurs during the processing of an existing interrupt, the new event may be lost. If the new interrupt event happens while the IRQ_Status Register 24 is being read (\overline{CE} is asserted), the event status bit may not be set and the \overline{IRQ} output will not stay asserted.	The application workaround is to use Freescale 802.15.4 software Version 1.051 or later, or to use Freescale SMAC Release 4.1 or later. For customers developing custom driver software, the second missing interrupt needs to be handled.
2	Some control bits do not default at reset to required values for best operation.	As part of the initialization procedure after a reset, there are mandatory register bits that must be written: <ol style="list-style-type: none"> 1. Register 0x08, Bit 1 set to 1. 2. Register 0x08, Bit 4 set to 1. 3. Register 0x11, Bits[9:8] set to 00. 4. Register 0x06, Bit 14 set to 1. The Freescale SMAC and the 802.15.4 MAC software incorporates these writes.



NOTES

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